

# DN74LS107

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## Dual J-K Flip-Flops (with Reset)

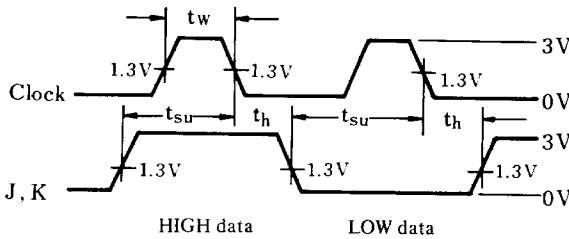
### Description

DN74LS107 contains two negative-edge triggered J-K flip-flop circuits, each with independent clock-CP, J, K, and direct-coupled reset input terminals.

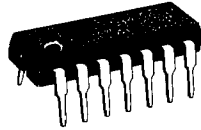
### Features

- Negative-edge trigger
- Independent input and output terminals for each flip-flop
- Direct-coupled reset inputs
- Q and  $\bar{Q}$  outputs
- Wide operating temperature range ( $T_a = -20$  to  $+75^\circ\text{C}$ )

### Timing definition



P-1



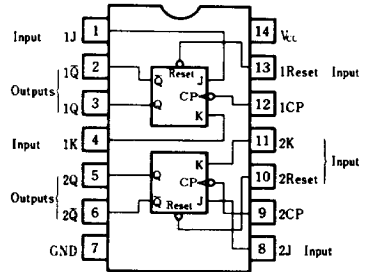
14-pin plastic DIL package

P-4



14-pin Pinflat package (SO-14D)

### Pin configuration (top view)



### Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$			-400	$\mu\text{A}$
	$I_{OL}$			8	mA
Operating temperature range	$T_{opr}$	-20	25	75	$^\circ\text{C}$
Clock frequency	$f_{clock}$	0		30	MHz
Pulse width	Clock High	$t_w$	20		ns
	Reset Low		25		ns
Set-up time	HIGH data	$t_{su}$	20 ↓		ns
	LOW data		20 ↓		ns
Hold time	$t_h$	0 ↓			ns

Notes 1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ( $T_a = -20 \sim +75^\circ\text{C}$ )

Parameter		Sym	Test conditions	Min	Typ*	Max	Unit
Input voltage		$V_{IH}$		2.0			V
		$V_{IL}$				0.8	V
Output voltage		$V_{OH}$	$V_{CC} = 4.75\text{V}$ , $V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}$ , $I_{OH} = -400\mu\text{A}$	2.7	3.4		V
		$V_{OL1}$	$V_{CC} = 4.75\text{V}$ $V_{IH} = 2\text{V}$		0.25	0.4	V
		$V_{OL2}$	$V_{IL} = 0.8\text{V}$ $I_{OL} = 8\text{mA}$		0.35	0.5	V
Input current	J-K	$I_{IH}$	$V_{CC} = 5.25\text{V}$ $V_I = 2.7\text{V}$			20	$\mu\text{A}$
	Reset					60	$\mu\text{A}$
	Clock					80	$\mu\text{A}$
	J-K	$I_{IL}$	$V_{CC} = 5.25\text{V}$ $V_I = 0.4\text{V}$			-0.4	mA
	Reset					-0.8	mA
	Clock					-0.8	mA
	J-K	$I_I$	$V_{CC} = 5.25\text{V}$ $V_I = 7\text{V}$			0.1	mA
	Reset					0.3	mA
	Clock					0.4	mA
Output short circuit current**		$I_{OS}$	$V_{CC} = 5.25$ $V_O = 0\text{V}$	-15		-100	mA
Input clamp voltage		$V_{IK}$	$V_{CC} = 4.75\text{V}$ $I_I = -18\text{mA}$			-1.5	V
Supply current***		$I_{CC}$	$V_{CC} = 5.25\text{V}$		4.0	8.0	mA

\* When constant at  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ .

\*\* Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

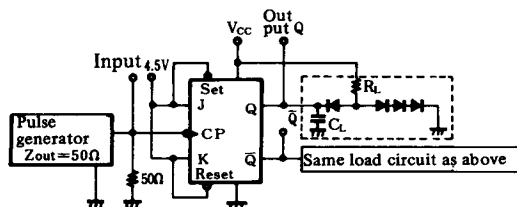
\*\*\* Measured with all outputs open, Q and  $\bar{Q}$  outputs alternately HIGH, and clock inputs grounded.■ Switching characteristics ( $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	$f_{\max}$			$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	30	45		MHz
Propagation delay time	$t_{PLH}$	Reset	Q, $\bar{Q}$			11	20	ns
	$t_{PHL}$	Clock				15	30	ns

\* Switching parameter measurement information

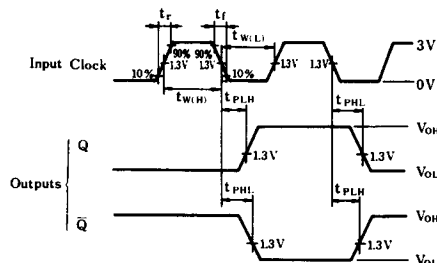
(1)  $f_{\max}$ ,  $t_{PLH}$ ,  $t_{PHL}$  (Clock  $\rightarrow$  Q,  $\bar{Q}$ )

## 1. Measurement circuit



1. Measurement made for each flip flop.
2.  $C_L$  includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

## 2. Waveforms

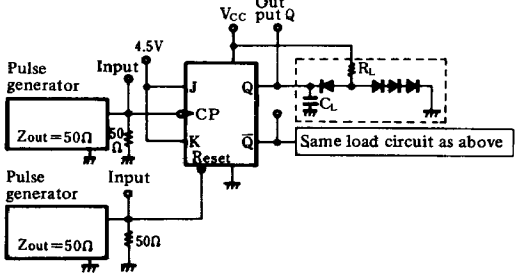


## Notes

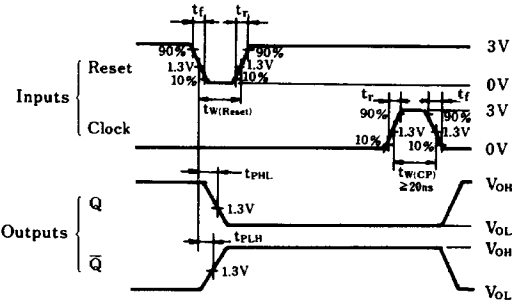
1. Clock input waveform:  $t_r \leq 15\text{ns}$ ,  $t_f \leq 6\text{ns}$ ,  
PRR = 1MHz,  
duty cycle = 50%.
2. When measuring  $f_{\max}$ ,  $t_r$  and  $t_f \leq 2.5\text{ns}$ .

[2]  $t_{PHL}(Reset \rightarrow Q)$ ,  $t_{PLH}(Set \rightarrow \bar{Q})$

1. Measurement circuit



2. Waveforms



- 1. Measurement made for each flip flop.
- 2.  $C_L$  includes probe and tool floating capacitance.
- 3. Diodes are all MA161.

Notes

- 1. Input waveform:  $t_r \leq 15ns$ ,  $t_f \leq 6ns$ ,  $PRR = 1MHz$ , duty cycle = 50%.

■ Truth tables

Inputs				Outputs	
Reset	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	$Q_0$	$\bar{Q}_0$

Notes

- 1. H: HIGH voltage level.
- 2. L: LOW voltage level.
- 3. ↓: Change from HIGH to LOW.
- 4. X: Either HIGH or LOW; doesn't matter.
- 5.  $Q_0$ : Q level prior to determination of input condition shown in table.
- 6.  $\bar{Q}_0$ :  $\bar{Q}$  level prior to determination of input condition shown in table.
- 7. Toggle: With ↓ change, outputs become compliment of previous condition.

■ Logic diagram (1/2)

