

HD74AC241/HD74ACT241

Octal Buffer/Line Driver with 3-State Output

HITACHI

ADE-205-382 (Z)

1st. Edition

Sep. 2000

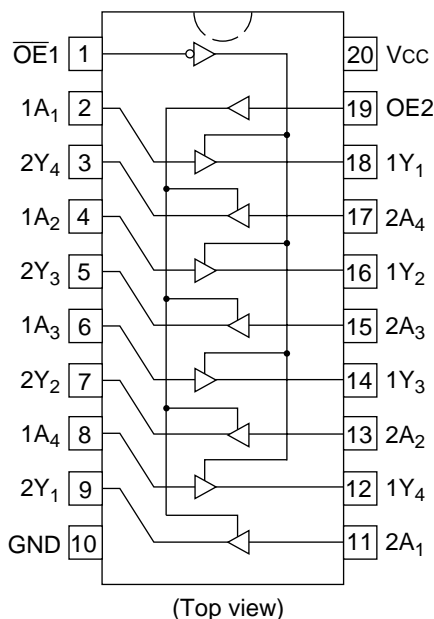
Description

The HD74AC241/HD74ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT241 has TTL-Compatible Inputs

Pin Arrangement



HD74AC241/HD74ACT241

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
OE ₁	A	Y
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE ₂	A	Y
H	L	L
H	H	H
L	X	Z

- H : High Voltage Level
L : Low Voltage Level
X : Immaterial
Z : High Impedance

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{CC}	80	μA	V _{IN} = V _{CC} or ground, V _{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I _{CC}	8.0	μA	V _{IN} = V _{CC} or ground, V _{CC} = 5.5 V, Ta = 25°C
Maximum additional I _{CC} /input (HD74ACT241)	I _{CCT}	1.5	mA	V _{IN} = V _{CC} – 2.1 V, V _{CC} = 5.5 V, Ta = Worst case

AC Characteristics: HD74AC241

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t _{PLH}	3.3	1.0	6.0	9.0	1.0	10.0	ns
Data to output		5.0	1.0	5.0	7.0	1.0	7.5	
Propagation delay	t _{PHL}	3.3	1.0	6.0	9.0	1.0	10.5	ns
Data to output		5.0	1.0	4.5	7.0	1.0	7.5	
Output enable time	t _{ZH}	3.3	1.0	6.5	12.5	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	9.5	
Output enable time	t _{ZL}	3.3	1.0	7.0	12.0	1.0	13.0	ns
		5.0	1.0	5.5	9.0	1.0	9.5	
Output disable time	t _{HZ}	3.3	1.0	8.0	12.0	1.0	12.5	ns
		5.0	1.0	6.5	10.0	1.0	10.5	
Output disable time	t _{LZ}	3.3	1.0	7.0	12.5	1.0	13.5	ns
		5.0	1.0	6.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT241

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t _{PLH}	5.0	1.0	6.5	9.0	1.0	10.0	ns
Data to output								
Propagation delay	t _{PHL}	5.0	1.0	7.0	9.0	1.0	10.0	ns
Data to output								
Output enable time	t _{ZH}	5.0	1.0	6.0	9.0	1.0	10.0	ns
Output enable time	t _{ZL}	5.0	1.0	7.0	10.0	1.0	11.0	ns
Output disable time	t _{HZ}	5.0	1.0	8.0	10.5	1.0	11.5	ns
Output disable time	t _{LZ}	5.0	1.0	7.0	10.5	1.0	11.5	ns

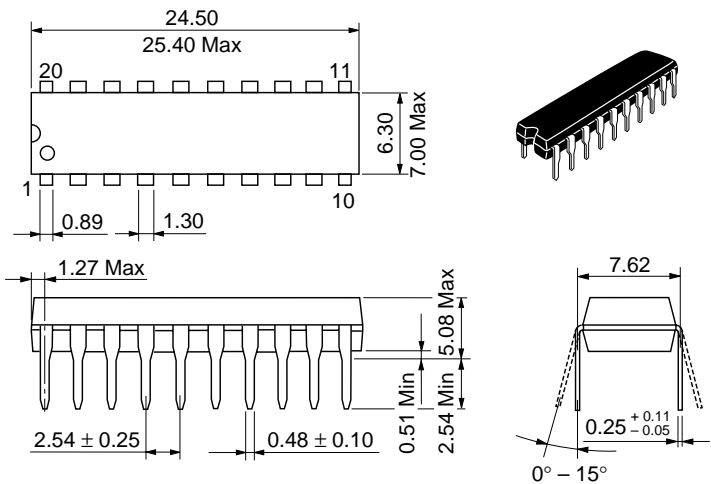
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	45.0	pF	V _{CC} = 5.0 V

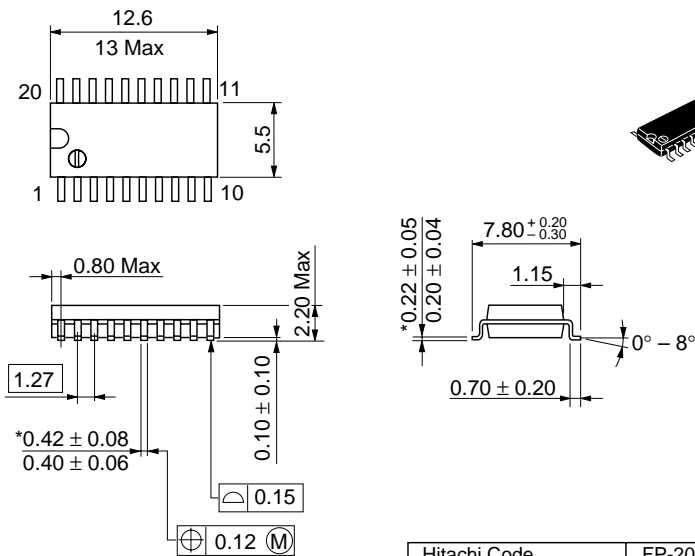
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

Unit: mm

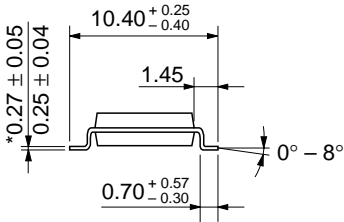
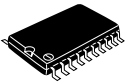
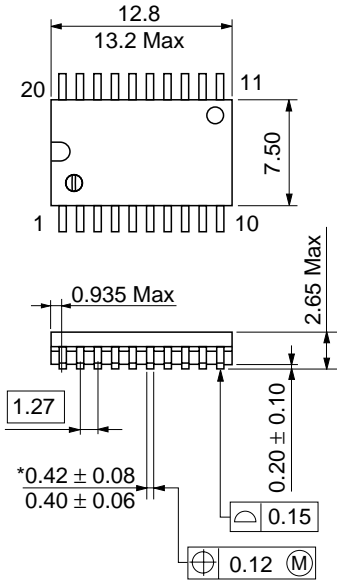


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

HD74AC241/HD74ACT241

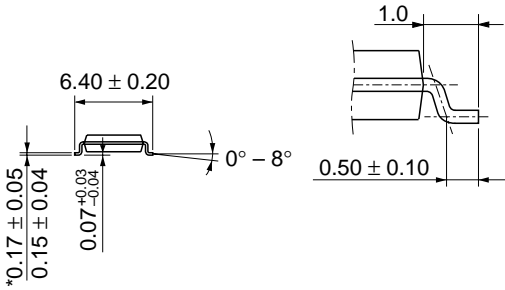
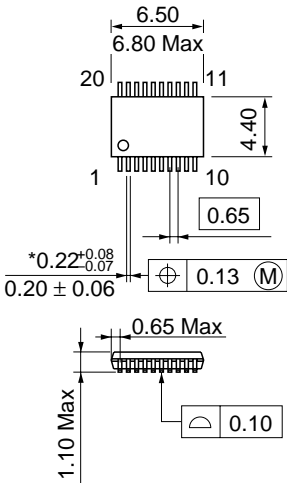
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.07 g

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