

**M66312P/FP****8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS****DESCRIPTION**

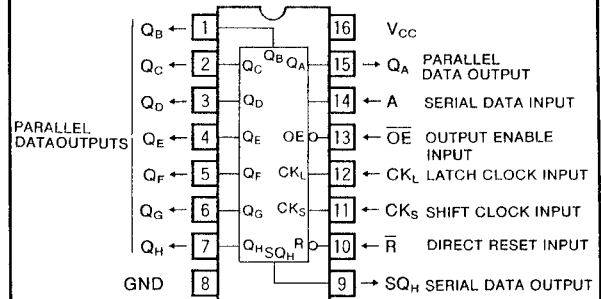
M66312 is a LED array driver having a 8-bit serial input and parallel output shiftregister function with 3-state output latch.

This product guarantees the output electric current of 16mA which is sufficient for LED drive, capable of flowing 8 bits continuously at the same time, and use either of cathode common LED and anode common LED.

In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

**FEATURES**

- High output current  $I_{OL}=16\text{mA}$ ,  $I_{OH}=-16\text{mA}$
- High speed (clock frequency) : 30MHz (typ)  
( $C_L=50\text{pF}$ ,  $V_{CC}=5\text{V}$ )
- Low power dissipation : 20μW/package (max)  
( $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$ , quiescent state)
- 3-state output (except serial data output)
- Wide operating temperature range :  $T_a=-40\sim+85^\circ\text{C}$

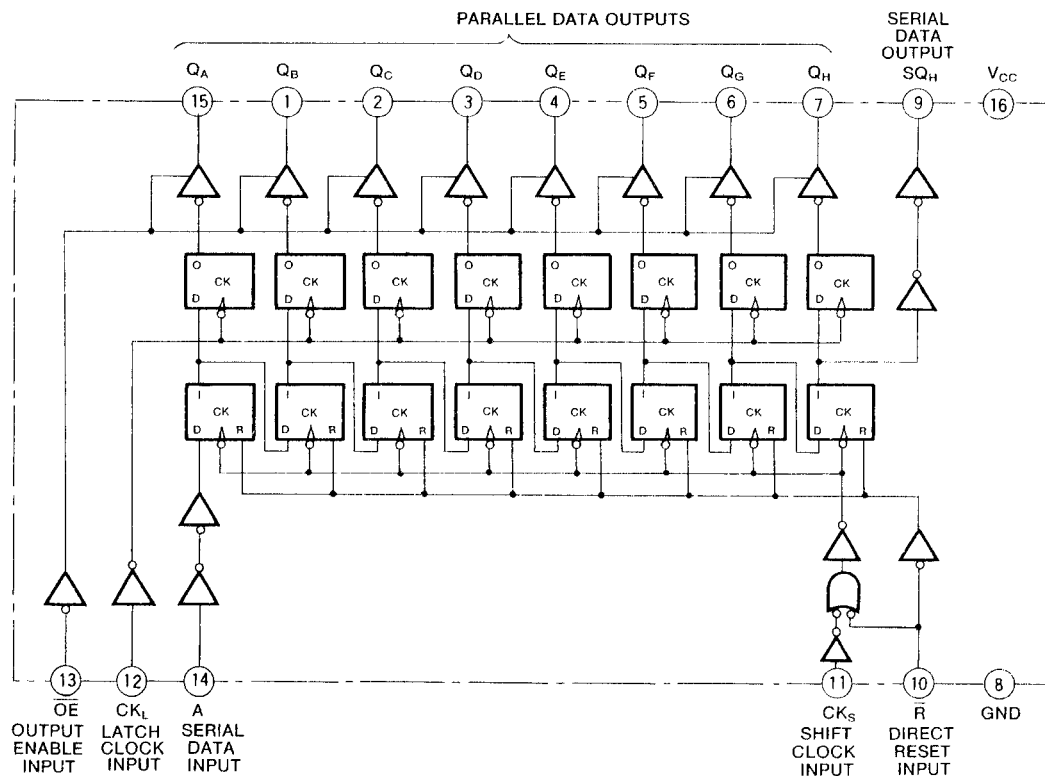
**PIN CONFIGURATION (TOP VIEW)**

Outline 16P4  
16P2N-A

**APPLICATION**

LED array drive of PRINTER

LED array drive of BUTTON TELEPHONE

**LOGIC DIAGRAM**

# 8-BIT LED DRIVER WITH SHIFTRREGISTER AND LATCHED 3-STATE OUTPUTS

## FUNCTIONAL DESCRIPTION

As M66312 uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftrregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input  $CK_S$  and latch clock input  $CK_L$  are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftrregister and the signal of A shifts shiting registers one by one when a pulse is impressed to  $CK_S$ . When A is "H", the signal of "H" shifts. When A is "L", the signal of "L" shifts.

When the pulse is impressed to  $CK_L$ , the contents of the

shifting register at that time are stored in a latching register, and they appear in the output from  $Q_A$  through  $Q_H$  are 3-state outputs.

To extend the number of bits, serial data output  $SQ_H$  is used to output the 8-bit of the shift register.

By connecting  $CK_S$  and  $CK_L$ , the shift register state delayed by 1 clock cycle is output at  $Q_A$  through  $Q_H$ .

When reset input  $\bar{R}$  is low, shift register and  $SQ_H$  will be reset. To reset  $Q_A$  through  $Q_H$  to low-level,  $CK_L$  must be changed from low-level to high-level after the shift register is reset by  $\bar{R}$ .

When output-enable input  $\overline{OE}$  is high,  $Q_A$  through  $Q_H$  will become high impedance state, but  $SQ_H$  is not changed. Even if  $\overline{OE}$  is changed, shift operation is not affected.

## FUNCTION TABLE (Note : 1)

Operation mode		Input					Parallel data output								Serial data output $SQ_H$
		$\bar{R}$	$CK_S$	$CK_L$	A	$\overline{OE}$	$Q_A$	$Q_B$	$Q_C$	$Q_D$	$Q_E$	$Q_F$	$Q_G$	$Q_H$	
Reset	Shift $t_1$	L	X	X	X	L	$Q_A^0$	$Q_B^0$	$Q_C^0$	$Q_D^0$	$Q_E^0$	$Q_F^0$	$Q_G^0$	$Q_H^0$	L
	Latch $t_2$	X	X	$\uparrow$	X	L	L	L	L	L	L	L	L	L	L
Shift latch operation	Shift $t_1$	H	$\uparrow$	X	H	L	$Q_A^0$	$Q_B^0$	$Q_C^0$	$Q_D^0$	$Q_E^0$	$Q_F^0$	$Q_G^0$	$Q_H^0$	$q_G^0$
	Latch $t_2$	H	X	$\uparrow$	X	L	H	$q_A^0$	$q_B^0$	$q_C^0$	$q_D^0$	$q_E^0$	$q_F^0$	$q_G^0$	$q_G^0$
	Shift $t_1$	H	$\uparrow$	X	L	L	$Q_A^0$	$Q_B^0$	$Q_C^0$	$Q_D^0$	$Q_E^0$	$Q_F^0$	$Q_G^0$	$Q_H^0$	$q_G^0$
	Latch $t_2$	H	X	$\uparrow$	X	L	L	$q_A^0$	$q_B^0$	$q_C^0$	$q_D^0$	$q_E^0$	$q_F^0$	$q_G^0$	$q_G^0$
3 state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	$q_H$

Note 1 :  $\uparrow$  : Change from low-level to high-level  
 $Q^0$  : Output state Q before  $CK_L$  changed  
X : Irrelevant  
 $q^0$  : Contents of shift register before  $CK_S$  changed  
q : Contents of shift register  
 $t_1, t_2$  :  $t_2$  is set after  $t_1$  is set  
Z : High impedance

**8-BIT LED DRIVER WITH SHIFTRREGISTER AND LATCHED 3-STATE OUTPUTS**

**ABSOLUTE MAXIMUM RATINGS** ( $T_a = -40 \sim +85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$-0.5 \sim +7.0$	V
$V_I$	Input voltage		$-0.5 \sim V_{CC} + 0.5$	V
$V_O$	Output voltage		$-0.5 \sim V_{CC} + 0.5$	V
$I_{IK}$	Input protection diode current	$V_I < 0\text{V}$	-20	mA
		$V_I > V_{CC}$	20	
$I_{OK}$	Output parasitic diode current	$V_O < 0\text{V}$	-20	mA
		$V_O > V_{CC}$	20	
$I_O$	Output current per output pin	$Q_A \sim Q_H$	$\pm 35$	mA
		$SQ_H$	$\pm 25$	
$I_{CC}$	Supply/GND current	$V_{CC}, \text{GND}$	$\pm 132$	mA
$P_d$	Power dissipation	(Note 2)	500	mW
$T_{stg}$	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

Note 2 : M66312FP ;  $T_a = -40 \sim +70^\circ\text{C}$ ,  $T_a = 70 \sim 85^\circ\text{C}$  are derated at  $-6\text{mW}/^\circ\text{C}$ .

**RECOMMENDED OPERATING CONDITIONS** ( $T_a = -40 \sim +85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$T_{opr}$	Operating temperature range	$-40$		$+85$	$^\circ\text{C}$
$t_r, t_f$	Input rising and falling time	$V_{CC}=4.5\text{V}$	0	500	ns
		$V_{CC}=5.5\text{V}$	0	400	

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=4.5 \sim 5.5\text{V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions		Limits				Unit
				T <sub>a</sub> =25℃			T <sub>a</sub> =-40~+85℃	
				Min	Typ	Max	Min	
V <sub>IH</sub>	High-level input voltage	V <sub>O</sub> = 0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>   = 20μA		0.70×V <sub>CC</sub>			0.70×V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	V <sub>O</sub> = 0.1V, V <sub>CC</sub> -0.1V  I <sub>O</sub>   = 20μA				0.30×V <sub>CC</sub>	0.30×V <sub>CC</sub>	V
V <sub>OH</sub>	High-level output voltage Q <sub>A</sub> ~Q <sub>H</sub>	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OH</sub> =-20μA	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V
		V <sub>CC</sub> =4.5V	I <sub>OH</sub> =-16mA	3.70 *		3.55 *		
V <sub>OH</sub>	High-level output voltage SQ <sub>H</sub>	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OH</sub> =-20μA	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		V
		V <sub>CC</sub> =4.5V	I <sub>OH</sub> =-4mA	4.0		3.9		
V <sub>OL</sub>	Low-level output voltage Q <sub>A</sub> ~Q <sub>H</sub>	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OL</sub> =20μA			0.1	0.1	V
		V <sub>CC</sub> =4.5V	I <sub>OL</sub> =16mA			0.7 *	0.85 *	
V <sub>OL</sub>	Low-level output voltage SQ <sub>H</sub>	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OL</sub> =20μA			0.1	0.1	V
		V <sub>CC</sub> =4.5V	I <sub>OL</sub> = 4 mA			0.4	0.5	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> =V <sub>CC</sub> , V <sub>CC</sub> =5.5V				0.1	1.0	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> =GND, V <sub>CC</sub> =5.5V				-0.1	-1.0	μA
I <sub>OZH</sub>	Off state high-level output current Q <sub>A</sub> ~Q <sub>H</sub>	V <sub>I</sub> =V <sub>IH</sub> , V <sub>IL</sub>	V <sub>O</sub> =V <sub>CC</sub>			1.0	10.0	μA
I <sub>OZL</sub>	Off state low-level output current Q <sub>A</sub> ~Q <sub>H</sub>	V <sub>CC</sub> =5.5V	V <sub>O</sub> =GND			-1.0	-10.0	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> =V <sub>CC</sub> , GND, V <sub>CC</sub> =5.5V				4.0	40.0	μA

\* : Limits of single PIN operating state

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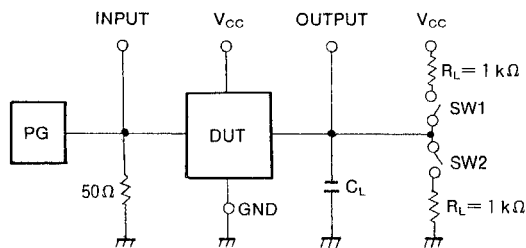
**SWITCHING CHARACTERISTICS** ( $V_{CC}=5V$ )

Symbol	Parameter	Test conditions	Limits					Unit
			T <sub>a</sub> =25℃			T <sub>a</sub> =-40~-+85℃		
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum clock frequency	C <sub>L</sub> =50pF	15			12		MHz
t <sub>PLH</sub>	Low-level to high-level and high-level to low-level output propagation time CKs-SQ <sub>H</sub>	C <sub>L</sub> =15pF (Note 3)			70		88	ns
t <sub>PHL</sub>	High-level to low-level output propagation time R̄-SQ <sub>H</sub>				70		88	ns
t <sub>PHL</sub>	High-level to low-level output propagation time R̄-SQ <sub>H</sub>				60		76	ns
t <sub>PLH</sub>	Low-level to high-level and high-level to low-level output propagation time CK <sub>L</sub> -Q <sub>A</sub> ~Q <sub>H</sub>	C <sub>L</sub> =50pF (Note 3)			60		76	ns
t <sub>PHL</sub>	Low-level to high-level and high-level to low-level output propagation time CK <sub>L</sub> -Q <sub>A</sub> ~Q <sub>H</sub>	(Note 3)			60		76	ns
t <sub>PLZ</sub>	Output disable time from low-level and high-level OE-Q <sub>A</sub> ~Q <sub>H</sub>	C <sub>L</sub> =5pF (Note 3)			50		64	ns
t <sub>PHZ</sub>	Output enable time from low-level and high-level OE-Q <sub>A</sub> ~Q <sub>H</sub>	(Note 3)			50		64	ns
t <sub>PZL</sub>	Output enable time to low-level and high-level OE-Q <sub>A</sub> ~Q <sub>H</sub>	C <sub>L</sub> =50pF (Note 3)			56		70	ns
t <sub>PZH</sub>	Output disable time to low-level and high-level OE-Q <sub>A</sub> ~Q <sub>H</sub>	(Note 3)			56		70	ns

**TIMING REQUIREMENTS** ( $V_{CC}=5V$ )

Symbol	Parameter	Test conditions	Limits					Unit
			T <sub>a</sub> =25℃			T <sub>a</sub> =−40~+85℃		
			Min	Typ	Max	Min	Max	
t <sub>w</sub>	CK <sub>S</sub> , CK <sub>L</sub> , $\bar{R}$ pulse width		32			40		ns
t <sub>su</sub>	A setup time with respect to CK <sub>S</sub>		40			50		ns
t <sub>su</sub>	CK <sub>S</sub> setup time with respect to CK <sub>L</sub>		40			50		ns
t <sub>h</sub>	A hold time with respect to CK <sub>S</sub>		10			10		ns
t <sub>rec</sub>	$\bar{R}$ recovery time with respect to CK <sub>S</sub>		20			26		ns

Note 3 : Test Circuit



Item	SW1	SW2
$t_{PLH}, t_{PHL}$	OPEN	OPEN
$t_{PLZ}$	CLOSE	OPEN
$t_{PHZ}$	OPEN	CLOSE
$t_{PZL}$	CLOSE	OPEN
$t_{PZH}$	OPEN	CLOSE

- (1) The pulse generator (PG) has the following characteristics (10%~90%) :  $t_r=6ns, t_f=6ns$
- (2) The capacitance  $C_L$  includes stray wiring capacitance and the probe input capacitance.

**8-BIT LED DRIVER WITH SHIFTREGISTER AND LATCHED 3-STATE OUTPUTS**

**TIMING DIAGRAM**

