

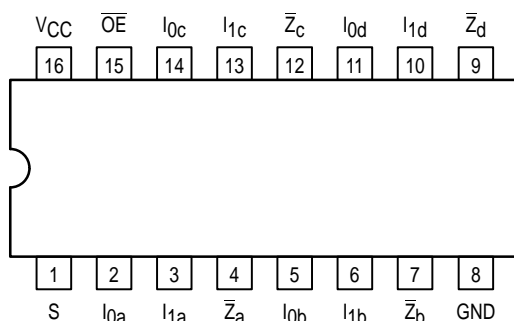


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

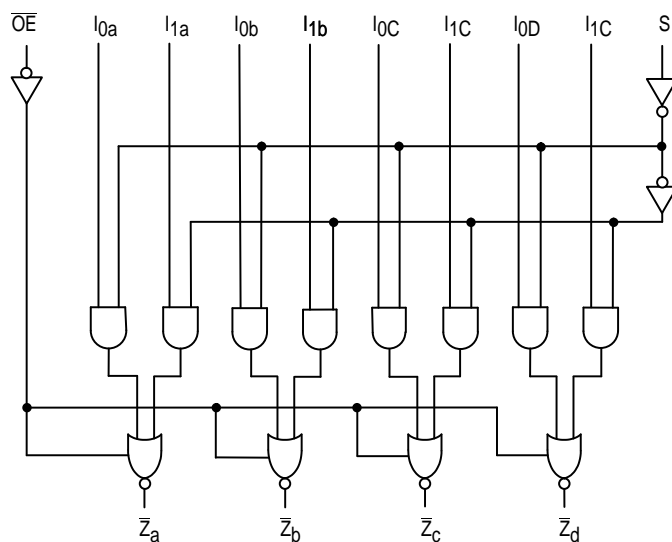
The MC74F258A is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common Data Select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs
- AC Enhanced Version of the F258

CONNECTION DIAGRAM (TOP VIEW)



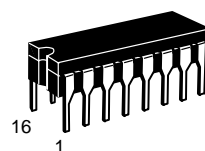
LOGIC DIAGRAM



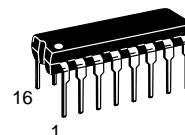
MC74F258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

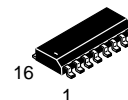
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

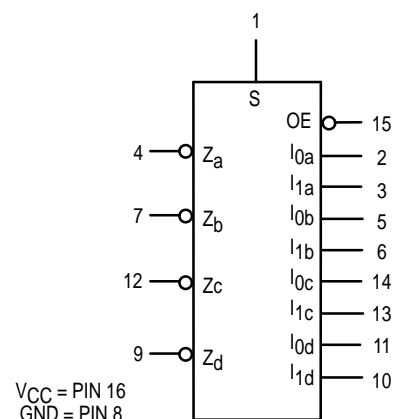


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXAJ Ceramic
MC74FXXXAN Plastic
MC74FXXXAD SOIC

LOGIC SYMBOL



MC74F258A

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
\overline{OE}	S	I ₀	I ₁	\overline{Z}
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High Impedance

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			−3.0	mA
I _{OL}	Output Current — Low	74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				−1.2	V	I _{IN} = −18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.7	3.3		V	I _{OH} = −3.0 mA	V _{CC} = 4.75 V
		74	2.4					V _{CC} = MIN
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH				50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW				−50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				−0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current			6.2	9.5	mA	S, I _{1X} = 4.5 V \overline{OE} , I _{0X} = GND	V _{CC} = MAX
I _{CCL}				15.1	23		I _{1X} = 4.5 V \overline{OE} , I _{0X} , S = GND	
I _{CCZ}				11.3	17		S, I _{0X} = GND \overline{OE} , I _{1X} = 4.5 V	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.

2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F258A

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	5.3	2.0	6.0	ns
t _{PHL}	I _n to \bar{Z}_n	1.0	4.0	1.0	5.0	
t _{PLH}	Propagation Delay	3.0	7.5	3.0	8.5	ns
t _{PHL}	S to \bar{Z}_n	2.5	7.0	2.5	8.0	
t _{PZH}	Output Enable Time	2.0	6.0	2.0	7.0	ns
t _{PZL}		2.5	7.0	2.5	8.0	
t _{PHZ}	Output Disable Time	2.0	6.0	2.0	7.0	ns
t _{PLZ}		1.5	6.0	1.5	7.0	

FUNCTIONAL DESCRIPTION

The F258A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\bar{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$\bar{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$\bar{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$\bar{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.