
HD74AC74

Dual D-Type Positive Edge-Triggered Flip-Flop

HITACHI

ADE-205-361 (Z)
1st. Edition
Sep. 2000

Description

The HD74AC74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Features

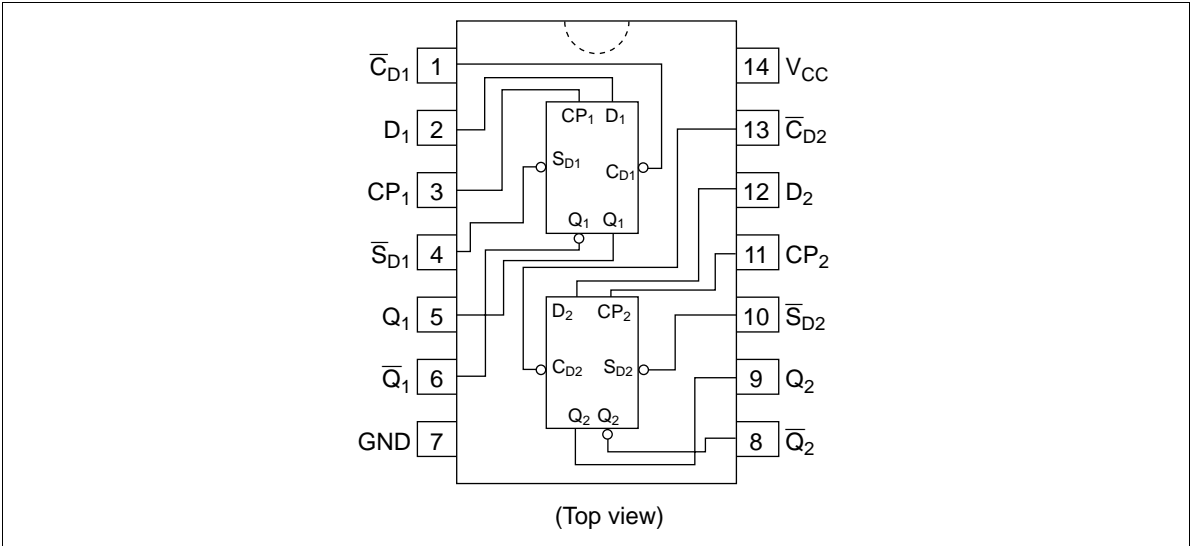
Asynchronous Inputs:

- Low input to \bar{S}_D (Set) sets Q to High level
- Low input to \bar{C}_D (Clear) sets Q to Low level
- Clear and Set are independent of clock
- Simultaneous Low on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} High

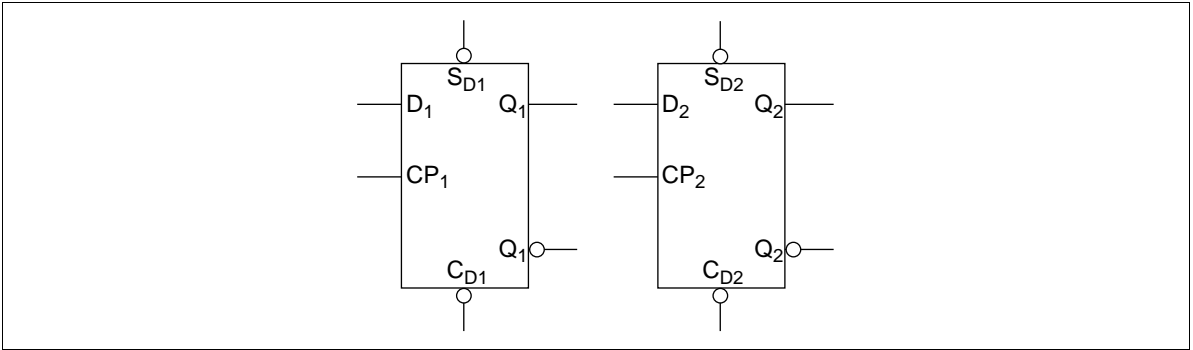
- Outputs Source/Sink 24 mA

HD74AC74

Pin Arrangement



Logic Symbol



Pin Names

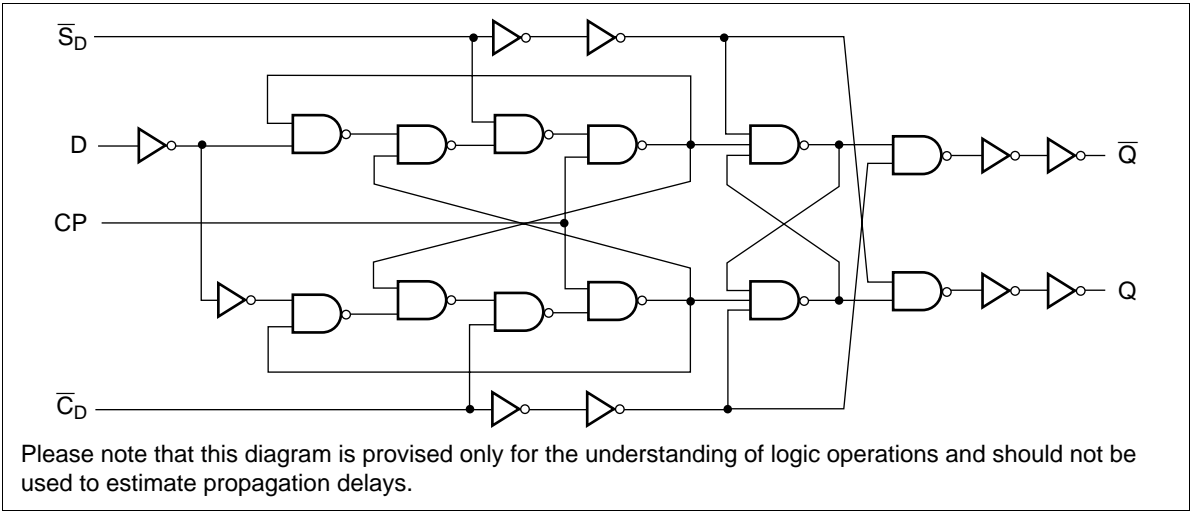
| | |
|--|---------------------|
| D_1, D_2 | Data Inputs |
| CP_1, CP_2 | Clock Pulse Inputs |
| $\overline{C}_{D1}, \overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}, \overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$ | Outputs |

Truth Table (Each Half)

| Inputs | | | | Outputs | |
|------------------|------------------|----------|---|---------|------------------|
| \overline{S}_D | \overline{C}_D | CP | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | \lceil | H | H | L |
| H | H | \lceil | L | L | H |
| H | H | L | X | Q_0 | \overline{Q}_0 |

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
 \lceil : Low-to-High Clock Transition
 Q_0 (\overline{Q}_0) : Previous Q (\overline{Q}) before Low-to-High Transition of Clock

Logic Diagram



DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|----------------------------------|----------|-----|---------|--|
| Maximum quiescent supply current | I_{CC} | 40 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$ |
| Maximum quiescent supply current | I_{CC} | 4.0 | μA | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$ |

AC Characteristics

| Item | Symbol | V _{CC} (V)*1 | Ta = +25°C C _L = 50 pF | | | Ta = −40°C to +85°C C _L = 50 pF | | Unit |
|---|------------------|-----------------------|--------------------------------------|------|------|---|------|------|
| | | | Min | Typ | Max | Min | Max | |
| Maximum clock frequency | f _{max} | 3.3 | 100 | 125 | — | 95 | — | MHz |
| | | 5.0 | 140 | 160 | — | 125 | — | |
| Propagation delay C _{Dn} or S _{Dn} to Q _n or Q _n | t _{PLH} | 3.3 | 1.0 | 8.0 | 12.0 | 1.0 | 13.0 | ns |
| | | 5.0 | 1.0 | 6.0 | 9.0 | 1.0 | 10.0 | |
| Propagation delay C _{Dn} or S _{Dn} to Q _n or Q _n | t _{PHL} | 3.3 | 1.0 | 10.5 | 12.0 | 1.0 | 13.5 | ns |
| | | 5.0 | 1.0 | 8.0 | 9.5 | 1.0 | 10.5 | |
| Propagation delay CP _n to Q _n or Q _n | t _{PLH} | 3.3 | 1.0 | 8.0 | 13.5 | 1.0 | 16.0 | ns |
| | | 5.0 | 1.0 | 6.0 | 10.0 | 1.0 | 10.5 | |
| Propagation delay CP _n to Q _n or Q _n | t _{PHL} | 3.3 | 1.0 | 8.0 | 14.0 | 1.0 | 14.5 | ns |
| | | 5.0 | 1.0 | 6.0 | 10.0 | 1.0 | 10.5 | |

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC74

| Item | Symbol | V _{CC} (V)*1 | Ta = +25°C C _L = 50 pF | | Ta = −40°C to +85°C C _L = 50 pF | | Unit |
|--|------------------|-----------------------|--------------------------------------|--------------------|---|--|------|
| | | | Typ | Guaranteed Minimum | | | |
| Set-up time, HIGH or LOW D _n to CP _n | t _{su} | 3.3 | 1.5 | 4.0 | 4.5 | | ns |
| | | 5.0 | 1.0 | 3.0 | 3.0 | | |
| Hold time, HIGH or LOW D _n to CP _n | t _h | 3.3 | −2.0 | 0 | 0 | | ns |
| | | 5.0 | −1.5 | 0 | 0 | | |
| CP _n or C _{Dn} or S _{Dn} Pulse width | t _w | 3.3 | 3.0 | 5.5 | 7.0 | | ns |
| | | 5.0 | 2.5 | 4.5 | 5.0 | | |
| Recovery time C _{Dn} or S _{Dn} to CP | t _{rec} | 3.3 | −2.5 | 0 | 0 | | ns |
| | | 5.0 | −2.0 | 0 | 0 | | |

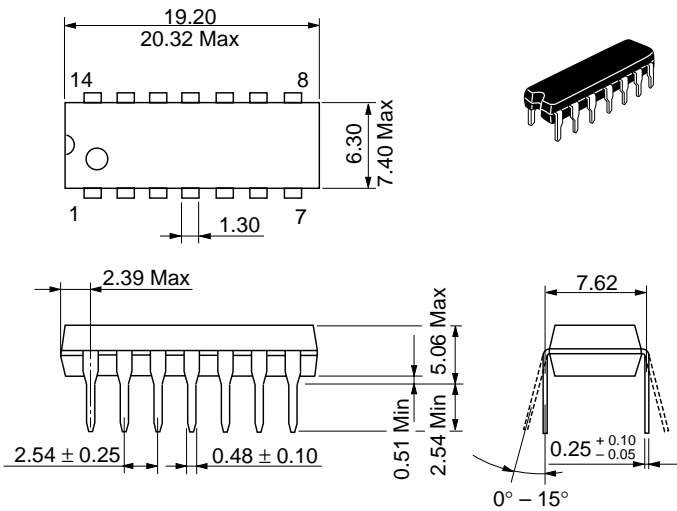
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

| Item | Symbol | Typ | Unit | Condition |
|-------------------------------|-----------------|------|------|-------------------------|
| Input capacitance | C _{IN} | 4.5 | pF | V _{CC} = 5.5 V |
| Power dissipation capacitance | C _{PD} | 35.0 | pF | V _{CC} = 5.0 V |

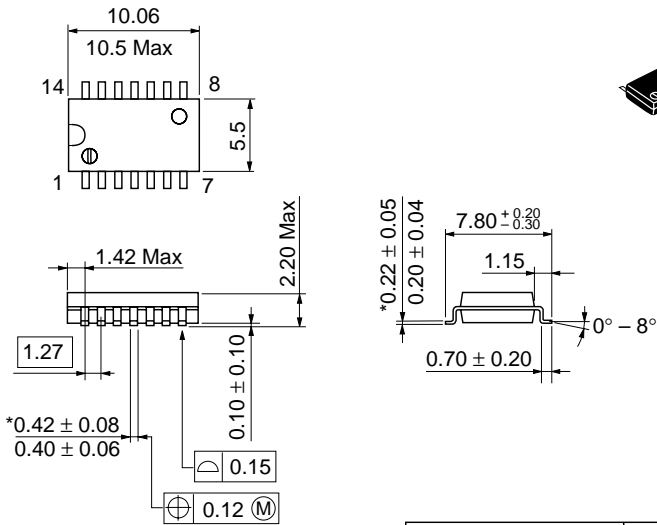
Package Dimensions

Unit: mm



| | |
|------------------------|----------|
| Hitachi Code | DP-14 |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.97 g |

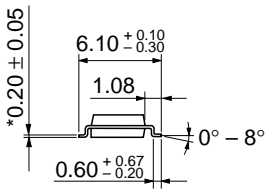
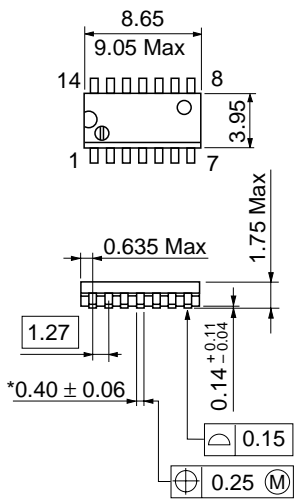
Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | FP-14DA |
| JEDEC | — |
| EIAJ | Conforms |
| Mass (reference value) | 0.23 g |

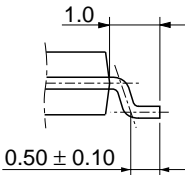
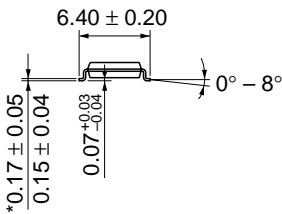
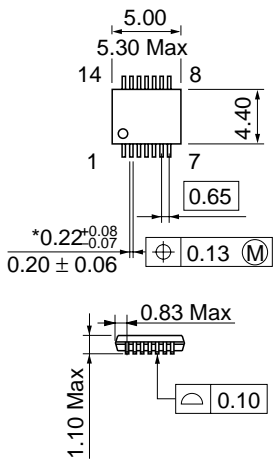
Unit: mm



*Pd plating

| | |
|------------------------|----------|
| Hitachi Code | FP-14DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.13 g |

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|---------|
| Hitachi Code | TTP-14D |
| JEDEC | — |
| EIAJ | — |
| Mass (reference value) | 0.05 g |

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